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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,387	09/27/2001	Jason E. Cosky	42390.P11979	2940

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,387	COSKY ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12,14-21 and 23-43* is/are rejected.

7)☒ Claim(s) *3,13 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 25, 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-12, 14-21, 23-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Franke (PGPUB: US 2001/0052054 A1).

Regarding claims 1, 4-5, 20, 23-24, 30, 34, 36 and 38, Franke discloses initializing a circuit, (one of References 101 in Figure 1; inherently the circuit is initialized as all circuits are initialized during power-up [reset] to a particular state), the circuit having at least one memory element coupled to a memory bus (comprised of local memory bus 111 and host memory bus 100 in Figure 1) on a host system; monitoring signals on the memory bus (Section 0054 – signals on the host memory bus are monitored) and detecting a first sequence of signals, the first sequence of

signals including a reserved memory address, wherein the reserved memory address comprises a particular memory address reserved for switching control of the at least one memory element and switching control of the at least one memory element to one of the circuit and the host (another one of References 101 in Figure 1) in response to detection of the reserved memory address, wherein switching control of the memory bus to one of the circuit and the host comprises a processing element in the circuit reading from or writing to the at least one memory element in the circuit (Section 0054-0055; the reserved memory addresses are the addresses assigned to each processor; when an address assigned to one of the processors is detected, control of the memory element via the local memory bus is switched to the processor assigned to have access to the memory region containing the assigned address).

Additionally with respect to claim 20, hardware system elements are intrinsically controlled by software such as device drivers, microcode, etc. and thus it is evident that the system above comprises a machine-accessible medium including instructions, that when executed by the machine, causes the machine to perform the operations above.

Regarding claims 2, 10, 21 and 37, detecting a second sequence of signals, the second sequence of signals including another reserved memory address (a memory request from a different one of References 101 in Figure 1) and switching control of the at least one memory element to the host system via the local memory bus in response to detection of the another reserved memory address, wherein switching control of the memory element to the host system comprises a processor on the host system reading from or writing to the at least one memory element in the circuit (Section 0054-0055).

Regarding claims 6 and 25, Franke discloses monitoring signals on the memory bus comprises the circuit monitoring control, address and data signals on the host system (Section 0054, Lines 8-11).

Regarding claims 7-8, 26-27 and 40, Franke discloses detecting a first sequence of signals comprises detecting at least one read/write signal to the reserved memory address (Section 0046).

Regarding claims 9 and 28, Franke discloses switching control of the memory bus to the circuit comprising a processing element in the circuit reading from or writing to the at least one memory element in the circuit (processor element within one of Reference 101).

Regarding claims 10 and 29, Franke discloses switching control of the memory element to the host system comprising a processor on the host system reading from or writing to the at least one memory element in the circuit (processor element within a different one of Reference 101).

Regarding claims 11, 14 and 32, Franke discloses a memory bus on the host system (Figure 1, Reference 100); a plurality of memory elements on a circuit, the plurality of memory elements (memory cells within Reference 111 in Figure 1) communicatively coupled with the memory bus (comprised of local memory bus 111 and host memory bus 100 in Figure 1); a processing element on the circuit communicatively coupled with the plurality of memory elements and the

memory bus (Figure 4, Reference 400), wherein the processing element monitors signals on the memory bus (Section 0054 - Section 0054 – signals on the host memory bus are monitored) and detecting a first sequence of signals, the first sequence of signals including a reserved memory address, wherein the reserved memory address comprises a particular memory address reserved for switching control of the at least one memory element and switching control of the at least one memory element to the circuit in response to detection of the reserved memory address (Section 0054-0055; the reserved memory addresses are the addresses assigned to each processor; when an address assigned to one of the processors is detected, control of the memory element via the local memory bus is switched to the processor assigned to have access to the memory region containing the assigned address).

Regarding claim 12, Franke discloses the processing element detecting a second sequence of signals, the second sequence of signals including another reserved memory address (a memory request from a different one of References 101 in Figure 1) and switching control of the at least one memory element to the host system in response to detection of the another reserved memory address, wherein switching control of the memory element to the host system comprises a processor on the host system reading from or writing to the at least one memory element in the circuit (Section 0054-0055).

Regarding claim 15, Franke discloses the processing element monitoring signals on the memory bus comprising the processing element monitoring control, address and data signals on the host system (Section 0054, Lines 8-11).

Regarding claims 16-19, Franke discloses the processing element detecting a read/write to the memory element (s)(Section 0046).

Regarding claims 31, 33, 35 and 39, Franke discloses the particular memory address comprising an address in a second memory (second memory partition) coupled with the memory bus (the second memory coupled to the bus is a second memory partition of Reference 111).
Regarding claim 41, Franke discloses the memory and the second processor comprising part of a single component (the single component is Figure 1, a data processing system).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Franke (PGPUB: 2001/0052054).

Franke does not explicitly disclose the memory comprising a SDRAM and does not disclose the single component comprising a DIMM coupled with the memory bus. However, it is well known in the art to use SDRAM memories, which provide fast memory access via burst mode operations and dual bank structure. Additionally, it is well known in the art to use DIMMs in a system to provide increased memory storage capacity. Hence, it would have been obvious to one

of ordinary skill in the art to provide theses features in the system taught by Franke for the desirable purpose of increased storage capacity and fast memory access.

Allowable Subject Matter

7. Claims 3, 13 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed have been fully considered but they are not persuasive. Regarding Applicant's argument that the circuit is not coupled to the memory bus, the Examiner disagrees. The circuit is coupled to the memory bus via the system bus and the memory controller (refer to Figures 1 and 4).

Applicant argues that Franke teaches monitoring signals on the system bus and then alleges that the system bus is not a memory bus. The bus relied upon in Franke's system functions the same as the bus in Applicant's invention. Applicant's host memory bus is coupled to I/O via chipset 230 in Figure 2. Additionally, the host memory bus transmits address, data and control signals as shown in Figure 3. Franke's bus also transmits address, data and control signals [refer to Franke section 0038]. As there appears to be no difference in the structure or the function of the buses, the mere fact that they are labeled different terms does not make them different.

Additionally the arbiter in Applicant's invention monitors the signals on the host memory bus [0020 in Applicant's specification], which is the same thing being performed in Franke's system.

Regarding Applicant's argument that Franke does not teach switching control of the memory element, the Examiner disagrees. Franke teaches that only one access is performed via the local memory bus at one time to avoid race conditions [refer to section 0040].

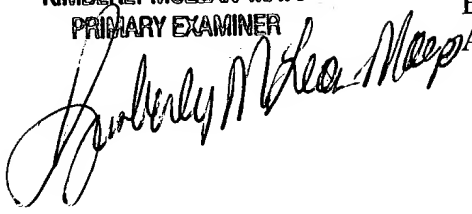
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M (10:00 - 6:30); Tues, Thr (10:00 - 4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER



Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

September 27, 2004